

# RF Power Field Effect Transistors

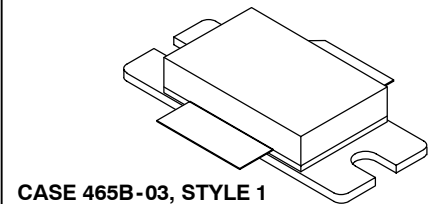
## N-Channel Enhancement-Mode Lateral MOSFETs

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

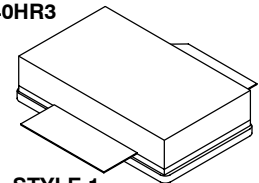
- Typical 2-carrier W-CDMA Performance:  $V_{DD} = 28$  Volts,  $I_{DQ} = 1200$  mA,  $P_{out} = 30$  Watts Avg., Full Frequency Band, Channel Bandwidth = 3.84 MHz, Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.  
Power Gain — 15.5 dB  
Drain Efficiency — 27.5%  
IM3 @ 10 MHz Offset — -37 dBc @ 3.84 MHz Channel Bandwidth  
ACPR @ 5 MHz Offset — -41 dBc @ 3.84 MHz Channel Bandwidth
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2140 MHz, 140 Watts CW Output Power
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched, Controlled Q, for Ease of Use
- Qualified Up to a Maximum of 32  $V_{DD}$  Operation
- Integrated ESD Protection
- Lower Thermal Resistance Package
- Designed for Lower Memory Effects and Wide Instantaneous Bandwidth Applications
- Low Gold Plating Thickness on Leads, 40 $\mu$ " Nominal.
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

**MRF6S21140HR3**  
**MRF6S21140HSR3**

**2170 MHz, 30 W AVG., 28 V**  
**2 x W-CDMA**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETs**



**CASE 465B-03, STYLE 1**  
**NI-880**  
**MRF6S21140HR3**



**CASE 465C-02, STYLE 1**  
**NI-880S**  
**MRF6S21140HSR3**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +68	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +12	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25 $^\circ\text{C}$	$P_D$	500 2.9	W W/ $^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	$T_J$	200	$^\circ\text{C}$
CW Operation	CW	140	W

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 80 $^\circ\text{C}$ , 140 W CW Case Temperature 75 $^\circ\text{C}$ , 30 W CW	$R_{\theta JC}$	0.35 0.38	$^\circ\text{C}/\text{W}$

1. MTF calculator available at <http://www.freescale.com/rf>. Select Tools/Software/Application Software/Calculators to access the MTF calculators by product.
2. Refer to AN1955/D, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

**NOTE - CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

**Table 4. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Off Characteristics</b>					
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 68\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{A}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{A}$
Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{A}$

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 300\ \mu\text{A}$ )	$V_{GS(th)}$	1	2	3	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_D = 1200\text{ mA}$ )	$V_{GS(Q)}$	2	2.8	4	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 3\text{ A}$ )	$V_{DS(on)}$	—	0.21	0.3	Vdc
Forward Transconductance ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 3\text{ A}$ )	$g_{fs}$	—	7.2	—	S

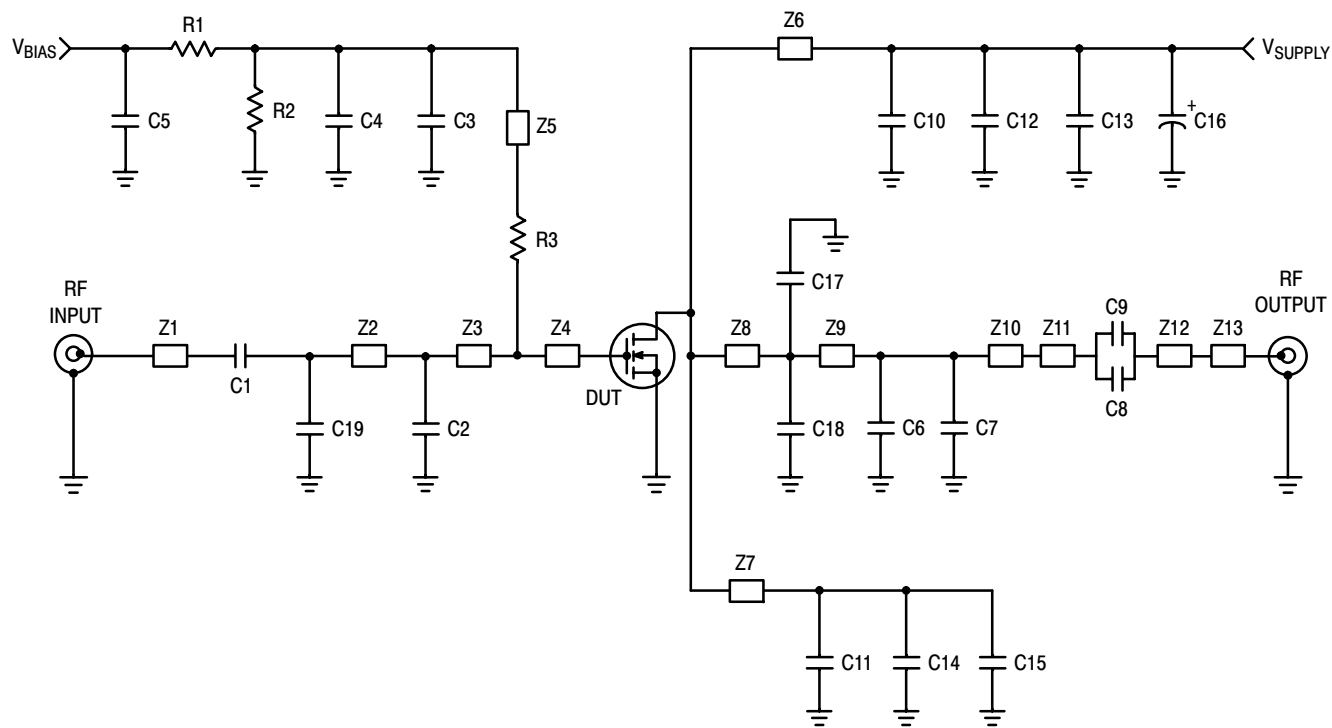
**Dynamic Characteristics** <sup>(1)</sup>

Reverse Transfer Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	2	—	pF
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**Functional Tests** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ} = 1200\text{ mA}$ ,  $P_{out} = 30\text{ W Avg.}$ ,  $f_1 = 2112.5\text{ MHz}$ ,  $f_2 = 2122.5\text{ MHz}$  and  $f_1 = 2157.5\text{ MHz}$ ,  $f_2 = 2167.5\text{ MHz}$ , 2-carrier W-CDMA, 3.84 MHz Channel Bandwidth Carriers. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset. IM3 measured in 3.84 MHz Channel Bandwidth @  $\pm 10\text{ MHz}$  Offset. Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.

Power Gain	$G_{ps}$	14.5	15.5	17.5	dB
Drain Efficiency	$\eta_D$	26	27.5	—	%
Intermodulation Distortion	IM3	—	-37	-35	dBc
Adjacent Channel Power Ratio	ACPR	—	-41	-38	dBc
Input Return Loss	IRL	—	-15	-9	dB

1. Part is internally matched both on input and output.



Z1	0.250" x 0.083" Microstrip	Z8	0.531" x 1.000" Microstrip
Z2	1.177" x 0.083" Microstrip	Z9	0.308" x 0.083" Microstrip
Z3	0.443" x 0.083" Microstrip	Z10	0.987" x 0.083" Microstrip
Z4	0.276" x 0.787" Microstrip	Z11, Z12	0.070" x 0.220" Microstrip
Z5	0.786" x 0.083" Microstrip (quarter wave length for bias purpose)	Z13	0.160" x 0.083" Microstrip
Z6, Z7	0.833" x 0.083" Microstrip (quarter wave length for supply purpose)	PCB	Taconic TLX8-0300, 0.030", $\epsilon_r = 2.55$

Figure 1. MRF6S21140HR3(HSR3) Test Circuit Schematic

Table 5. MRF6S21140HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C3, C8, C9, C10, C11	6.8 pF 100B Chip Capacitors	100B6R8CW	ATC
C2	0.8 pF 100B Chip Capacitor	100B0R8BW	ATC
C4	220 nF Chip Capacitor (1812)	1812Y224KXA	Vishay - Vitramon
C5, C12, C13, C14, C15	10 $\mu$ F Chip Capacitors (2220)	C5750X5R1H106MT	TDK
C6, C19	0.2 pF 100B Chip Capacitors	100B0R2BW	ATC
C7	0.5 pF 100B Chip Capacitor	100B0R5BW	ATC
C16	220 $\mu$ F, 63 V Electrolytic Capacitor, Radial	13668221	Philips
C17, C18	0.1 pF 100B Chip Capacitors	100B0R1BW	ATC
R1, R2	10 k $\Omega$ , 1/4 W Chip Resistors (1206)		
R3	10 $\Omega$ , 1/4 W Chip Resistor (1206)		

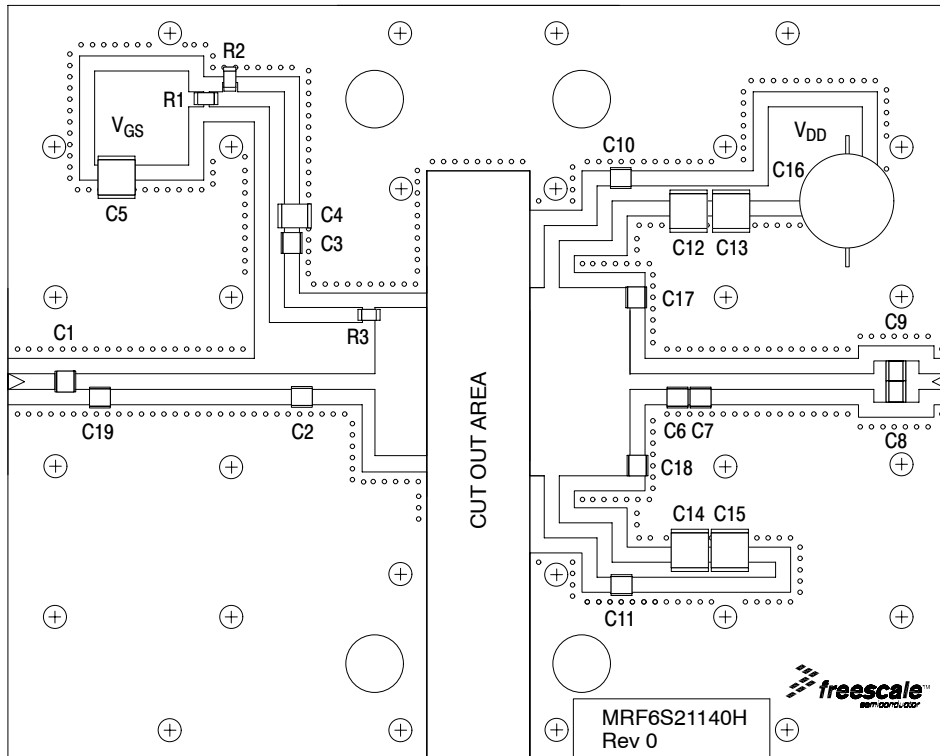
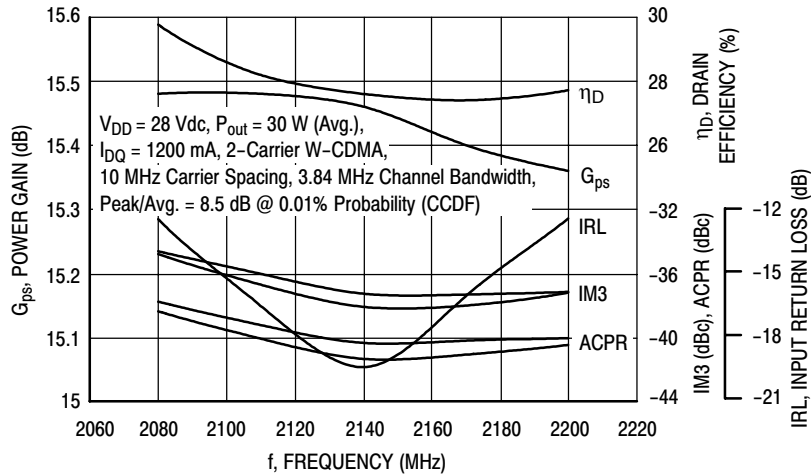
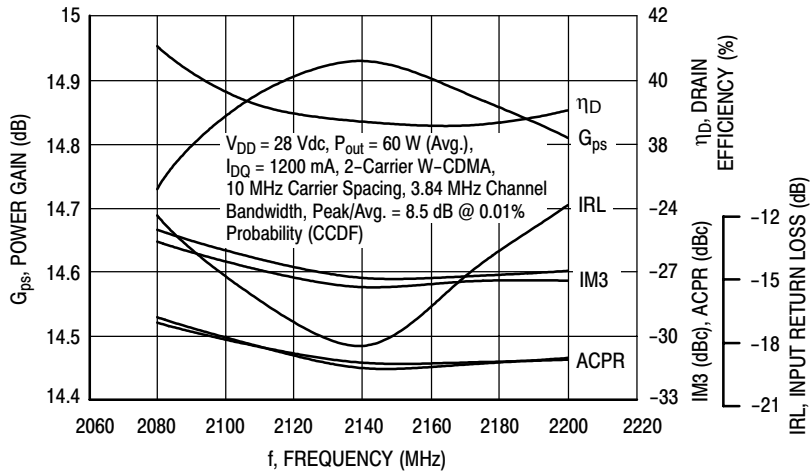


Figure 2. MRF6S21140HR3(HSR3) Test Circuit Component Layout

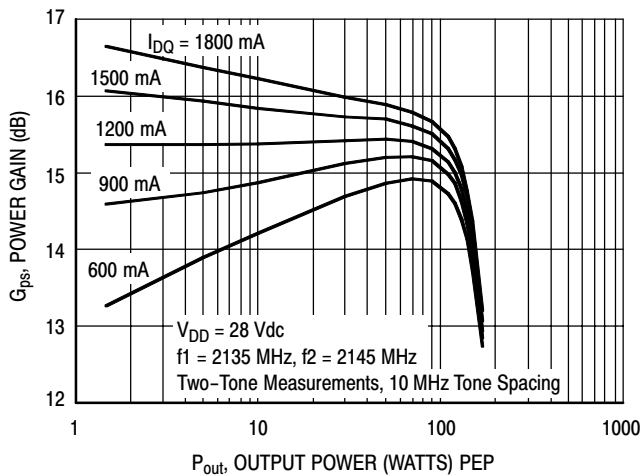
## TYPICAL CHARACTERISTICS



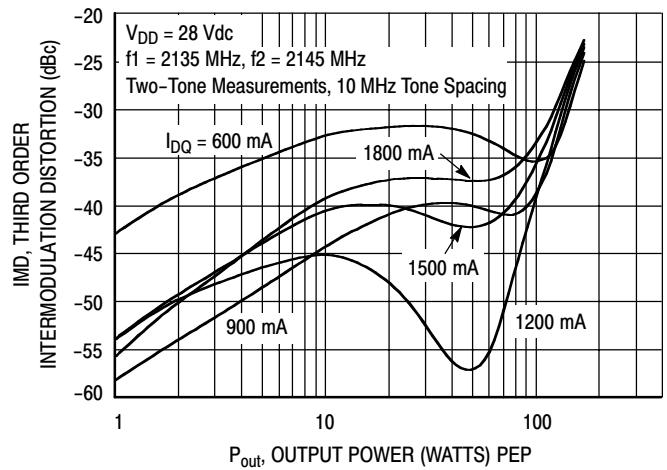
**Figure 3. 2-Carrier W-CDMA Broadband Performance @  $P_{out} = 30$  Watts Avg.**



**Figure 4. 2-Carrier W-CDMA Broadband Performance @  $P_{out} = 60$  Watts Avg.**

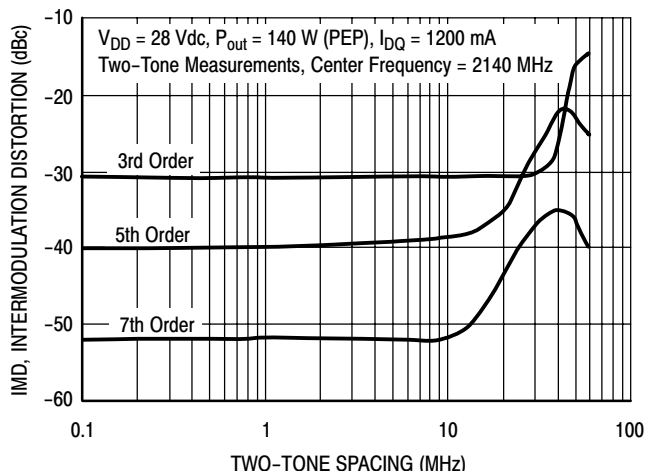


**Figure 5. Two-Tone Power Gain versus Output Power**

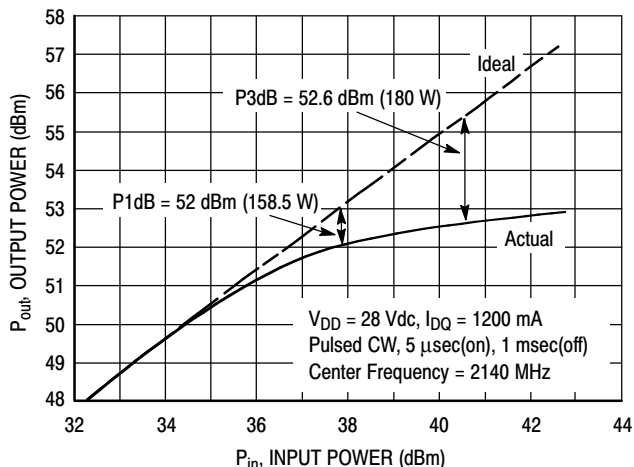


**Figure 6. Third Order Intermodulation Distortion versus Output Power**

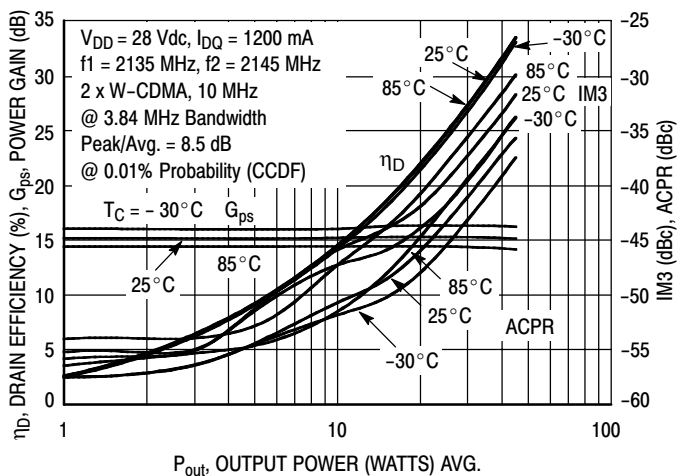
## TYPICAL CHARACTERISTICS



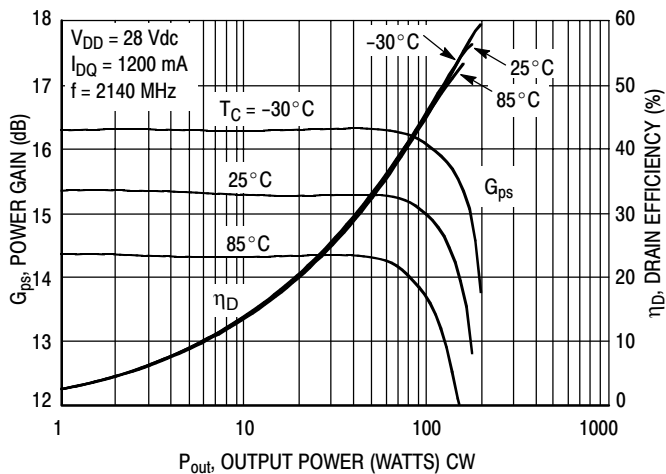
**Figure 7. Intermodulation Distortion Products versus Tone Spacing**



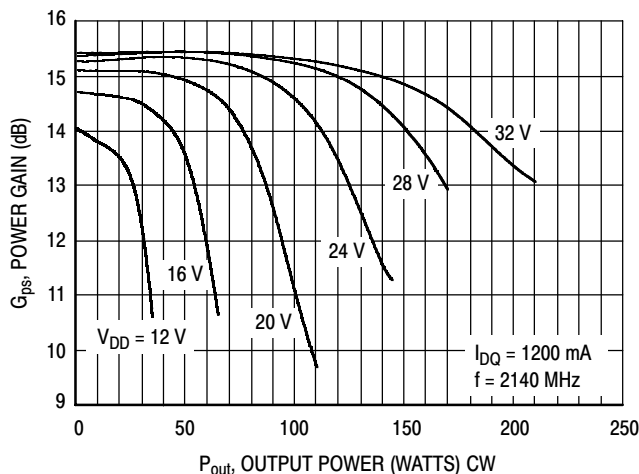
**Figure 8. Pulse CW Output Power versus Input Power**



**Figure 9. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power**

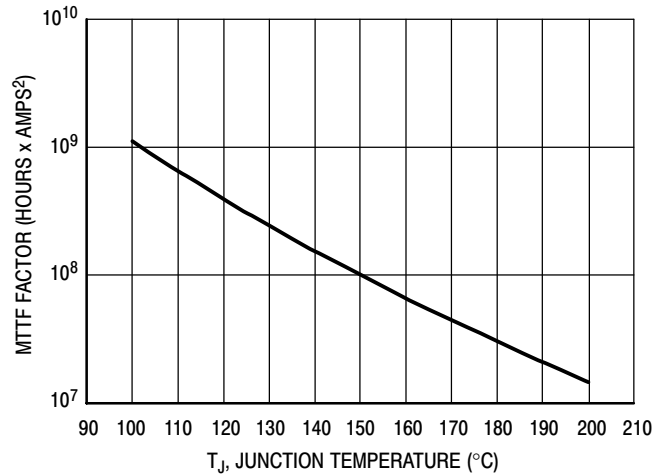


**Figure 10. Power Gain and Drain Efficiency versus CW Output Power**



**Figure 11. Power Gain versus Output Power**

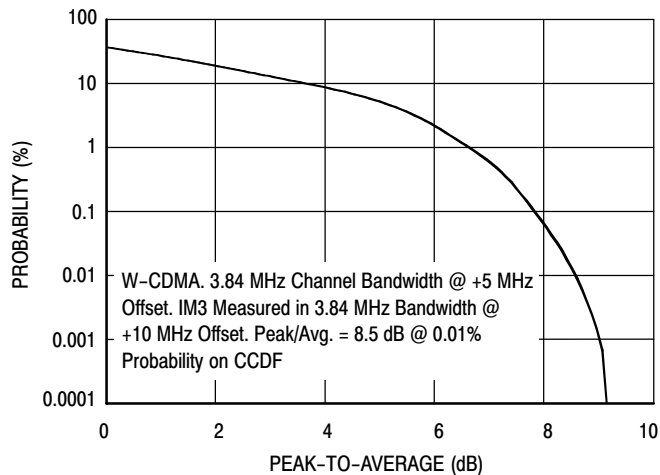
## TYPICAL CHARACTERISTICS



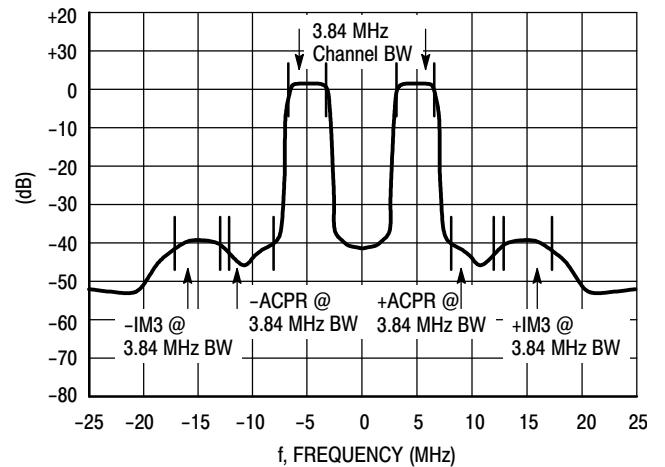
This above graph displays calculated MTTF in hours x ampere<sup>2</sup> drain current. Life tests at elevated temperatures have correlated to better than  $\pm 10\%$  of the theoretical prediction for metal failure. Divide MTTF factor by  $I_D^2$  for MTTF in a particular application.

**Figure 12. MTTF Factor versus Junction Temperature**

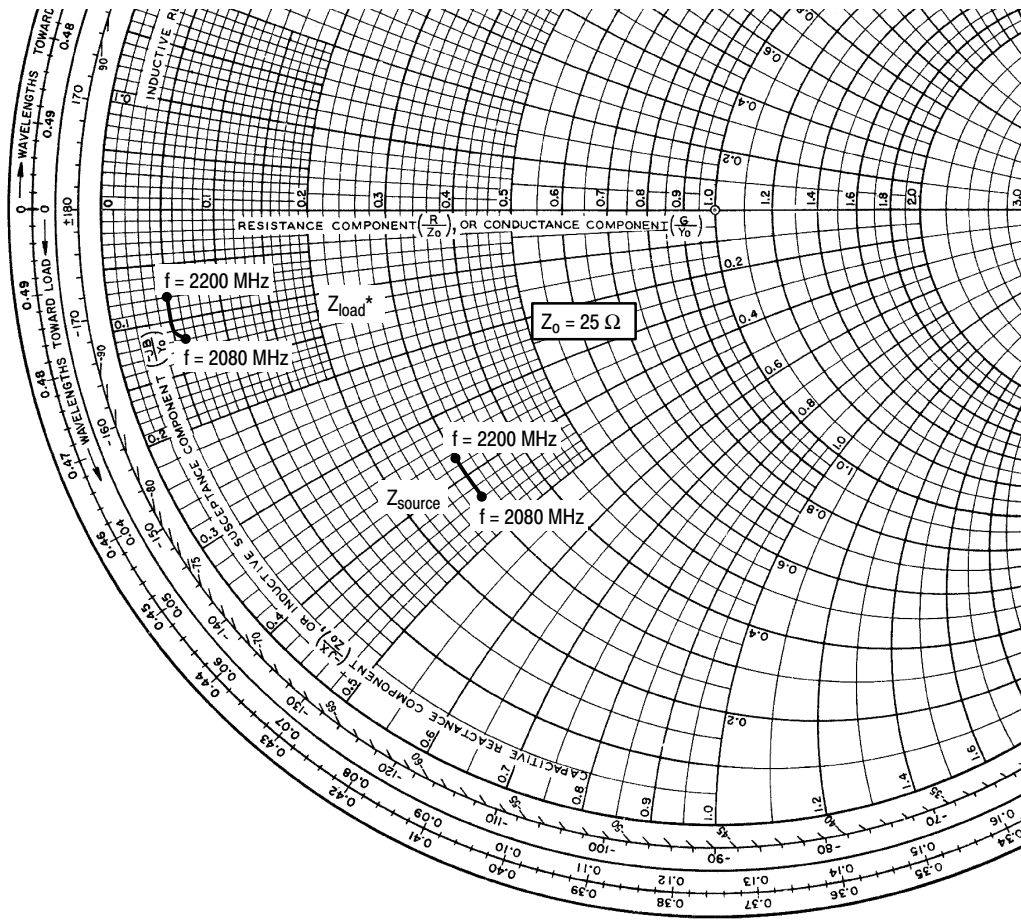
## TYPICAL CHARACTERISTICS W-CDMA TEST SIGNAL



**Figure 13. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 67% Clipping, Single-Carrier Test Signal**



**Figure 14. 2-Carrier W-CDMA Spectrum**



$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 1200 \text{ mA}$ ,  $P_{out} = 30 \text{ W Avg.}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
2080	$7.53 - j10.99$	$1.40 - j3.03$
2110	$7.57 - j10.67$	$1.37 - j2.78$
2140	$7.58 - j10.23$	$1.34 - j2.52$
2170	$7.51 - j9.73$	$1.32 - j2.28$
2200	$7.44 - j9.32$	$1.31 - j2.06$

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

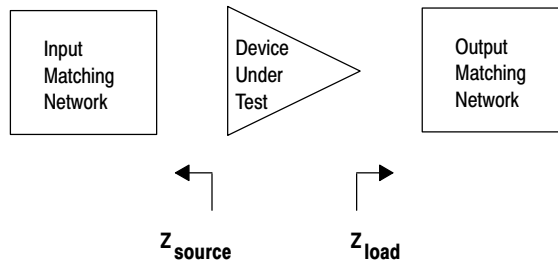


Figure 15. Series Equivalent Source and Load Impedance

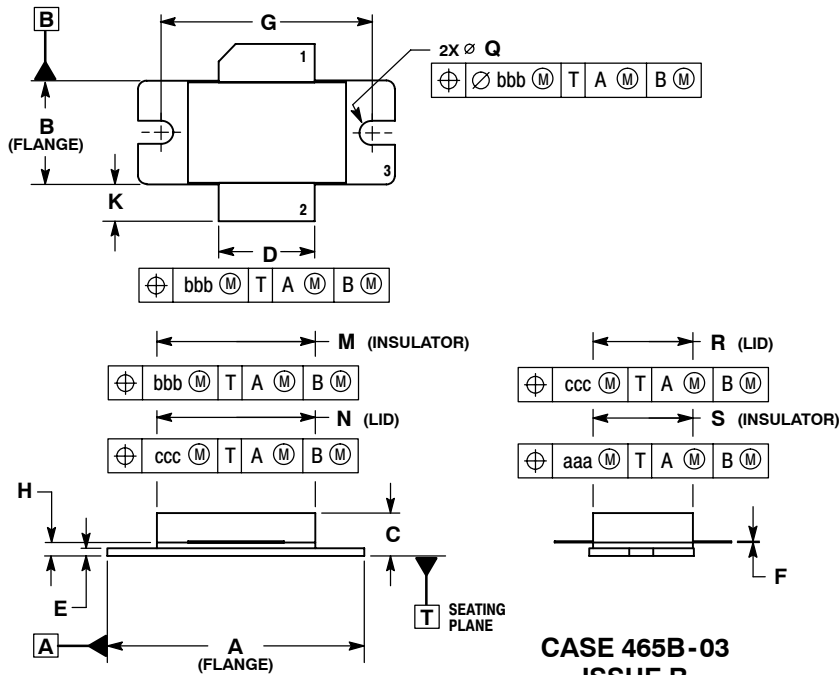


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# NOTES

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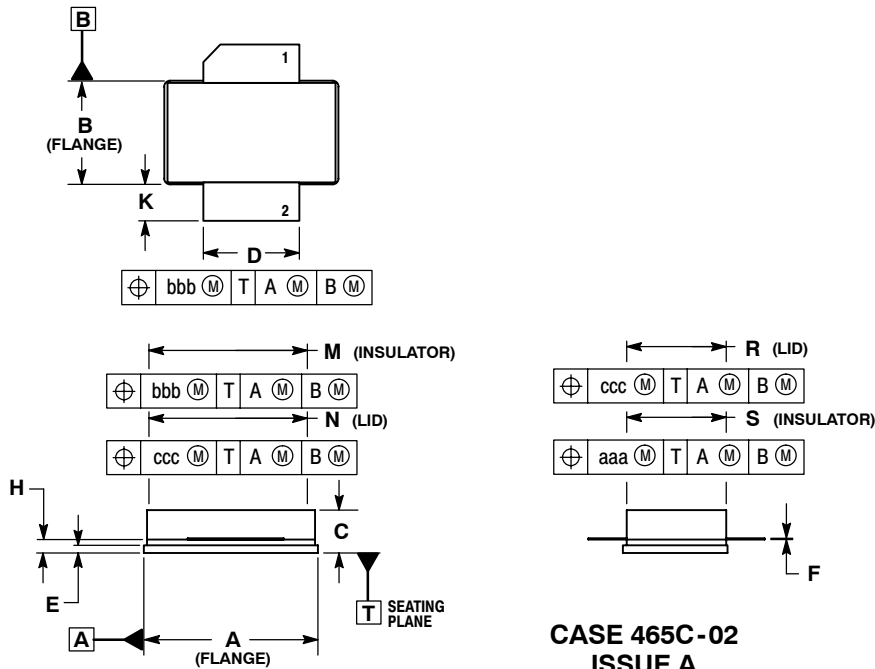
## PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
  4. DELETED

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.535	0.545	13.6	13.8
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
Q	∅.118	∅.138	∅3.00	∅3.51
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:  
 PIN 1. DRAIN  
 2. GATE  
 3. SOURCE



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
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  3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.905	0.915	22.99	23.24
B	0.535	0.545	13.60	13.80
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:  
 PIN 1. DRAIN  
 2. GATE  
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